9.4 A 40GHz DLL-Based Clock Generator in 90nm CMOS Technology

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The multiphase delay-locked loop (MDLL) is widely used for clock deskewing, clock generation and digital transceivers in serial links. To realize a high-frequency MDLL-based clock multiplier [1], one can increase the input frequency and the number of delay cells. However, several limitations should be investigated. Increasing the input frequency of the MDLL impacts the accuracy of the phase detector (PD), the matching between the up/down charge-pump currents, and the bandwidth requirement of the delay cells in a voltage-controlled delay line (VCDL). The number of delay cells in an MDLL determines the multiplication factor of an MDLL-based clock multiplier. Once the delay cell is selected in a given process, its intrinsic delay is determined. Increasing the number of delay cells also increases the total intrinsic delay. When the total intrinsic delay of a VCDL is greater than one input clock period, the MDLL will be harmonic-locked. Owing to the intrinsic delay, the trade-off between the operation frequency and the number of delay cells exists in a conventional MDLL. It also limits the output frequency of a MDLL-based clock multiplier.

A multi-period-locked DLL that solves the above problems is shown in Fig. 9.4.1. It consists of a conventional DLL with M delay cells, a start-controlled circuit, two divide-by-N dividers, and a duty-cycle correction (DCC) array. A DLL with an additional LC-tank edge combiner is used to generate the multiplied clock. The operation principle of the proposed multi-period-locked DLL is explained using the special case of $N = 2$, where N is the divider ratio. The timing diagram is shown in Fig. 9.4.2. When the 'Start' signal is active, the internal clock, CK_{in}, and the output clock, CK_{vcdl}, of the VCDL are divided by two. Then, the divide-by-2 outputs are connected to the start-controlled circuit. The start-controlled circuit is composed of four DFFs and two AND gates, as shown in Fig. 9.4.1. The clock, CK_{p2}, is enabled by the DFF3 and AND gate; then the 'UP' signal is activated to raise the controlled voltage, decreasing the delay of the VCDL to minimum. The dummy DFF4 is used to match the delay. The clock, CK_{p1}, is enabled after two periods of the clock, CK_{N1}, by using the DFF1, DFF2 and the AND gate. This ensures the multi-period-locked DLL locks from the minimal delay to avoid the harmonic locking [2]. When the multi-period-locked DLL is locked, the total delay of the VCDL is NT_{REF} $(=2\ T_{REF})$, where T_{REF} is the period of the internal clock. In general, let us select the number of the delay cells in the VCDL to be M. Assume that N and M are co-prime. For Fig. 9.4.1, the output phase of every delay cell with respect to the internal clock is expressed as

$$\left(\frac{jN}{M}-\left[\frac{jN}{M}\right]\right)\cdot T_{REF},\ \mathrm{j}=1\sim\mathrm{M}\quad M,N,j\in N \qquad (1)$$

where [ ] denotes the Gauss symbol. Although the monotonic phase relation among the delay cells does not hold, the multi-phase characteristics still exist. For example, in a conventional MDLL, if $N = 1$and $M = 9$ in eq. (1), the output phases of the nine delay cells is

$$\frac{1}{9}T_{REF},\frac{2}{9}T_{REF},\frac{3}{9}T_{REF},\frac{4}{9}T_{REF},\frac{5}{9}T_{REF},\frac{6}{9}T_{REF},\frac{7}{9}T_{REF},\frac{8}{9}T_{REF},\frac{9}{9}T_{REF} \qquad (2)$$

In the multi-period-locked DLL, if N =2 and $M = 9$, the output phases of the nine delay cells is

$$\frac{2}{9}T_{REF},\frac{4}{9}T_{REF},\frac{6}{9}T_{REF},\frac{8}{9}T_{REF},\frac{1}{9}T_{REF},\frac{3}{9}T_{REF},\frac{5}{9}T_{REF},\frac{7}{9}T_{REF},\frac{9}{9}T_{REF} \qquad (3)$$

Although the phase sequence is not monotonic, the multi-phase characteristics still exist. To have the monotonic phase outputs, the output buffers can be appropriately routed to achieve.

The design of a 40GHz clock multiplier by using the proposed DLL with $N = 2$ and $M = 9$ is described as follows. Since the divide-by-2 divider is adopted, the accuracy and match requirements for the PD and charge pump are relaxed. The conventional PD and charge pump in [1] are adopted. The VCDL is composed of nine pseudo-differential delay cells, as shown in Fig. 9.4.3(a). The cross-coupled pair M3-M4 is used to increase the swing. The PMOS transistors, M7-M8, adjust the delay and the PMOS transistors, M5-M6, act as the active load. For this DLL to work properly, the maximal delay $T_{d,\max}$ and the minimal delay $T_{d,\min}$ of the VCDL should satisfy the following constraint

$$\mathrm{T}_{d,\max} \geq NT_{REF} \geq T_{d,\min} \qquad (4)$$

By using the start-controlled circuit and divide-by-N dividers, the limitation between the intrinsic delay and the number of the delay cells is relaxed since the VCDL could be locked within multiple periods. In this case, it needs two periods. The phase blending technique [3] is adopted to in the DCC array to ensure the output clock has 50% duty cycle. To realize a 40GHz clock generator, the LC-tank edge combiner [1] with a symmetrical inductor is used, as shown in Fig. 9.4.3(b). A symmetrical inductor of 1.1nH is designed by using a commercial electromagnetic tool. Simulation results show that there is an amplitude decrement of 11% at the output of LC-tank edge combiner if this inductor has a variation ±5%. To reduce the required number of the pads, a 10-to-1 multiplexer is used to measure sequentially the multiphase outputs of the proposed DLL.

This chip is been fabricated in a 90nm CMOS process. Figure 9.4.4 shows the die micrograph and the core area is $0.374\times0.326\mathrm{mm}^2$. The supply voltage is 1V, and the power consumption of the whole chip is 45mW. Figure 9.4.5 shows the measured the nine multiphase outputs (9.4mV/div) for the DLL at an input frequency of 5GHz. The measured rms and peak-to-peak jitters are 0.874ps and 7.56ps, respectively, as shown in Fig. 9.4.6(a). The measured input frequency range is from 2 to 5GHz. To realize a 40GHz clock generator, an LC-tank edge combiner is adopted [1]. Figure 9.4.6(b) shows the measured output spectrum of 40GHz where input frequency of the proposed DLL is 4.4445GHz. The measured phase noise is -86dBc/Hz at an offset frequency of 600kHz. Fig. 9.4.7 shows the performance summary and comparisons with the previous works.

Acknowledgement:
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References:

[1] G. Chien and P.R. Gray, "A 900MHz Local Oscillator Using a DLL-Based Frequency Multiplier Technique for PCS Applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1995-1996, Dec., 2000.
[2] H.H. Chang, J.W. Lin, C.Y. Yang, and S.I. Liu, "A Wide Range Delay-Locked Loop with a Fixed Latency of One Clock Cycle," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1021-1027, Aug., 2002.
[3] K. Nakamura, M. Fukaishi, Y. Hirota, et al., "A CMOS 50% Duty Cycle Repeater Using Complementary Phase Blending," *Symp. VLSI Circuits*, pp. 48-49, Jun., 2000.
[4] T.C. Lee and K.J. Hsiao, "The Design and Analysis of a DLL-Based Frequency Synthesizer for UWB Application," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1245-1252, Jun., 2006.

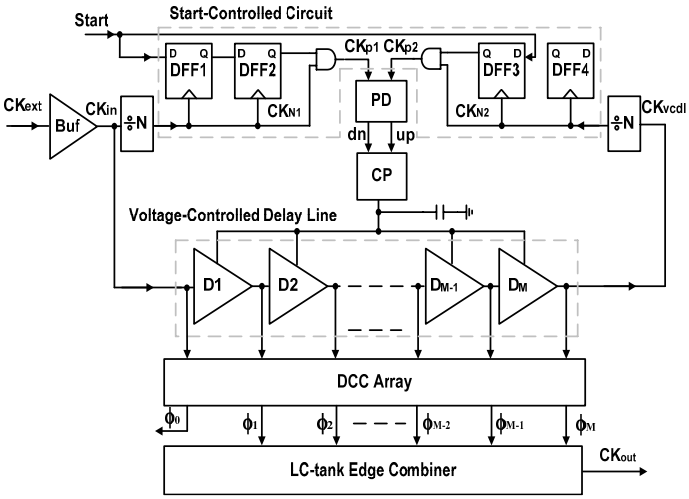

Figure 9.4.1: The proposed multi-period-locked DLL.

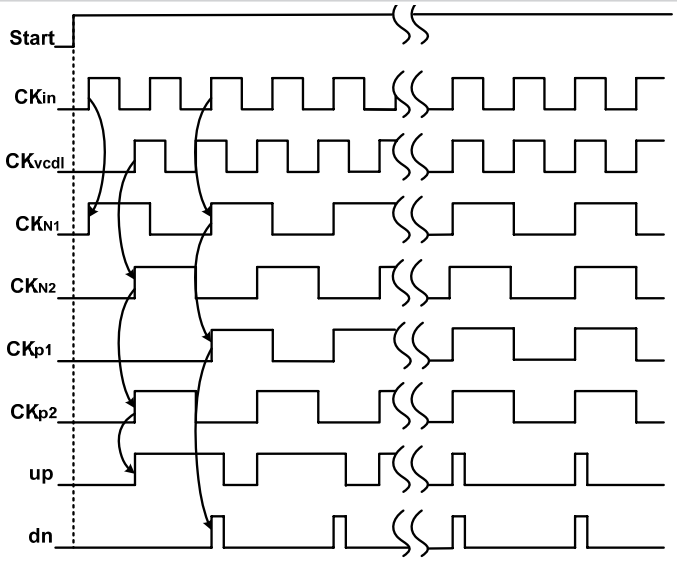

Figure 9.4.2: The simplified timing diagram of the proposed DLL when N = 2.

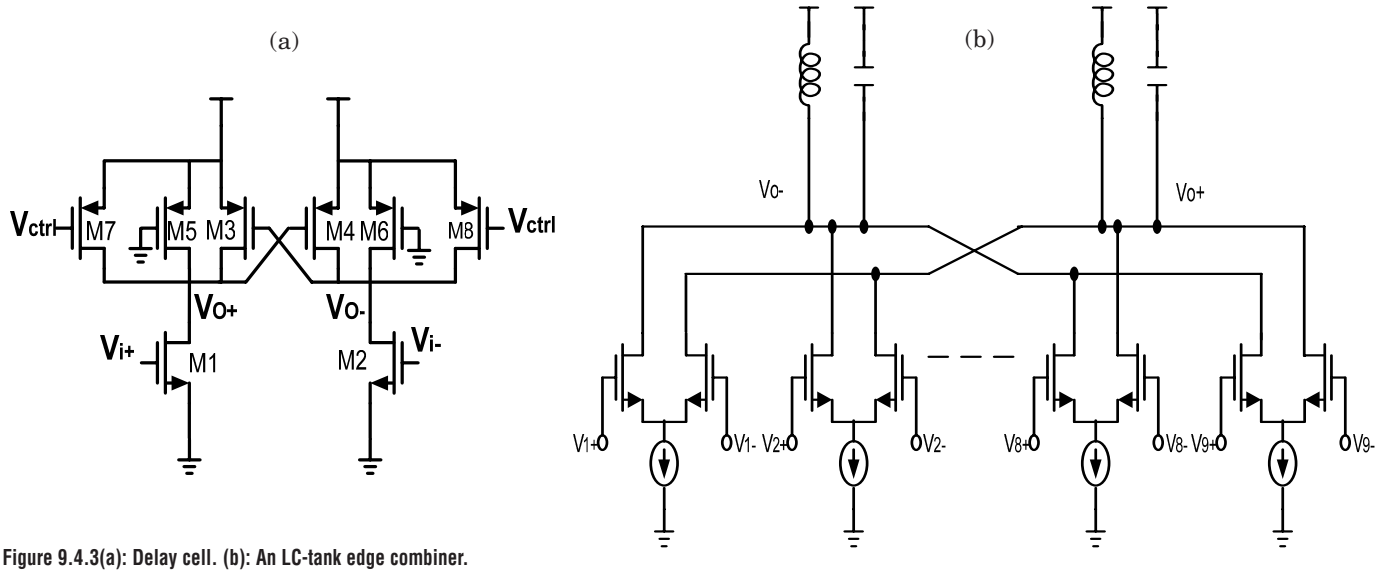

Figure 9.4.3(a): Delay cell. (b): An LC-tank edge combiner.

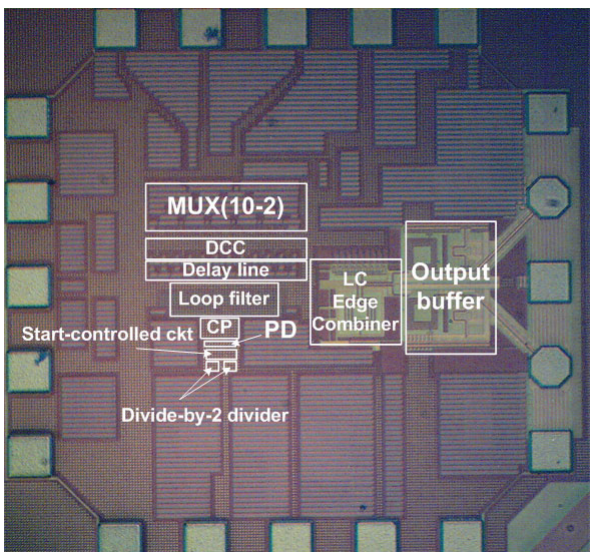

Figure 9.4.4: Die micrograph.

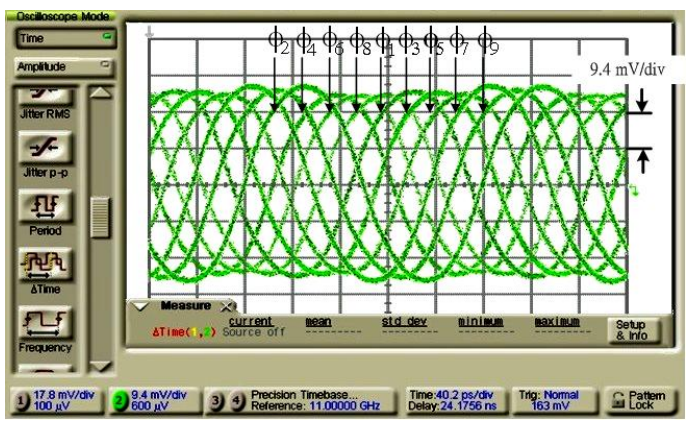

Figure 9.4.5: The measured multiphase outputs of the proposed DLL at 5GHz.

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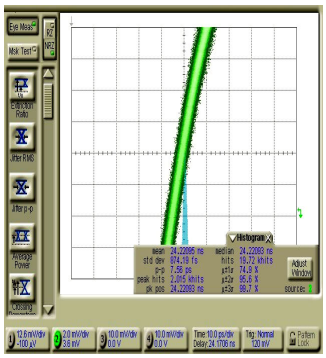
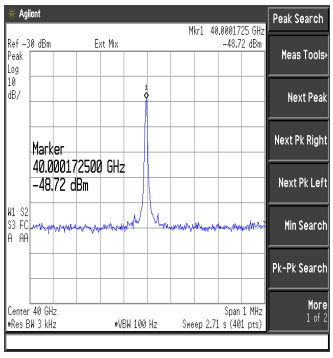


(a)



(b)

Figure 9.4.6: (a) the measured jitter of the DLL at 5GHz. (b) The measured output spectrumof a 40GHz clock generator using the proposed DLL.

	This work	[1]	[4]
Process	0.09μm	0.35μm	0.18μm
Supply	1V	3.3V	1.8V
Power	45mW	130mW	22mW
Input frequency	2-5GHz	100MHz	528MHz
Multi-phase count	9	9	17
Peak-peak jitter	7.56ps@5GHz	X	X
rms jitter	0.874ps@5GHz	X	X
Output frequency	40GHz	900MHz	8.976GHz
Phase noise	86dBc/Hz@600kHz	118dBc/Hz @600kHz	120dBc/Hz @1MHz
Core area	0.374×0.326 mm^2	1.2×1mm^2	0.88×0.6 mm^2

Figure 9.4.7: Performance comparisons with the previous works.

